**SDRAMController Module Description Document**

**1. Introduction**  
SDRAM refers to Synchronous Dynamic Random-Access Memory.

Synchronous means that the SDRAM operates in sync with a clock signal, and the SDRAM Controller sends commands, reads data, and writes data based on this synchronous clock.

Dynamic means the memory array requires continuous refreshing to ensure data is not lost.

Random means the SDRAM Controller can freely specify an address to read from or write to the SDRAM.

**2. Main Features**

  One SDRAM interface.

  Supports 8-bit, 9-bit, and 10-bit column addresses; 11-bit, 12-bit, and 13-bit row addresses.

  Supports 2 banks and 4 banks.

**3. Configuration Procedure**  
When using SDRAM on the AP80 development board, all jumpers and jumper wires on connectors P2 and P7 must be removed.

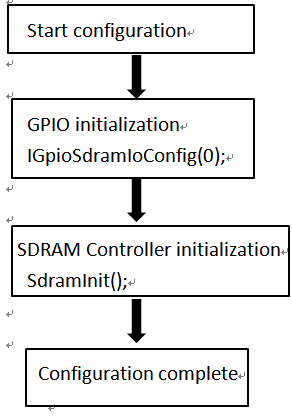


Figure 1 SDRAM configuration flow